wherein said non-volatile memory sets the setting of a second set value to said second register means as a necessary condition for enabling erase and programming operations, and

said CPU sets a value other than the second set value to said second register means upon said branch and sets the second set value to said second register means for each return from the branch.

A1 cont.

5. (Amended) The microcomputer according to claim 1, further including an interrupt control circuit for inputting an interrupt request signal therein, and performing arbitration of interrupt requests which compete with one another, and an interrupt priority level-based interrupt mask process to thereby output an interrupt signal to said CPU, and

wherein said CPU causes said interrupt control circuit to carry out a setting for masking an interrupt lower in interrupt priority level than a non-maskable interrupt.

A2

9. (Amended) The microcomputer according to claim 7, further including a RAM disposed in an address space of said CPU, and

A3

wherein said non-volatile memory has a transfer control program for transferring the erase and program control program to said RAM, and said CPU sets parameters for said another process to the erase and program control program transferred to said RAM, based on the set value of the first register means and thereby executes the erase and program control program.

A3 cont.

Please add the following claims:

40. (New) The microcomputer according to claim 2, further including second register means (FKEY) readable and writable by said CPU, and

A4

wherein said non-volatile memory sets the setting of a second set value to said second register means as a necessary condition for enabling erase and programming operations, and

said CPU sets a value other than the second set value to said second register means upon said branch and sets the second set value to said second register means for each return from the branch.

41. (New) The microcomputer according to claim 40, wherein the value other than the second set value is code information indicative of the progress of an erase and program process.

42. (New) The microcomputer according to claim 2, further including an interrupt control circuit for inputting an interrupt request signal therein, and performing arbitration of interrupt requests which compete with one another, and an interrupt priority level-based interrupt mask process to thereby output an interrupt signal to said CPU, and

wherein said CPU causes said interrupt control circuit to carry out a setting for masking an interrupt lower in interrupt priority level than a non-maskable interrupt.

43. (New) The microcomputer according to claim 42, wherein said CPU executes a process for changing the location of an interrupt process routine for a non-maskable interrupt request to an address of a RAM upon execution of the erase and programming.

44. (New) The microcomputer according to claim 8, further including a RAM disposed in an address space of said CPU, and

wherein said non-volatile memory has a transfer control program for transferring the erase and program control program to said RAM, and said CPU sets parameters for said another process to the erase and program control program transferred to said RAM, based on the set value of the first register means and thereby executes the erase and program control program.